

METHOD OF FORMING INTER-DIELECTRIC LAYER IN SEMICONDUCTOR DEVICE

5 BACKGROUND OF THE INVENTION

Field of the Invention:

The invention relates generally to a method of forming an interlayer
10 dielectric film in a semiconductor device, and more particularly to, a method
of forming an interlayer dielectric film in a semiconductor device capable of
easily burying an insulating material even between metal lines having a narrow
gap without voids, in a process of burying the insulating material between the
metal lines in order to electrically insulate them.

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Description of the Prior Art:

As a next-generation DRAM is developed, the length of a MOSFET
channel used is significantly reduced and the minimum pitch size of word lines
and bit lines is also gradually reduced. In a multi-layer metal structure
20 system such as DRAM, further, a method by an insulating spacer is formed on
the sidewall of a metal line using nitride or oxide in order to insulate the metal
line and a metal plug, has been widely used, which further reduces the distance
between the metal lines. In this case, upon deposition of IMD (inter metal
dielectric is deposition), a gap filling comes to the front as a serious problem.

Fig. 1 shows a layout of a general 8F2 DRAM after the word lines and the bit lines are formed, Figs. 2A ~ 2C are cross-sectional views of the device taken along lines A-A', B-B' and C-C' in Fig. 1, and Figs. 3A ~ 3C are cross-sectional views of the device taken along lines A-A', B-B' and C-C' in Fig. 1.

5 Referring now to Fig. 1, Figs. 2A ~ 2C and Figs. 3A ~ 3C, a word line 13, a word line spacer 14, a first interlayer dielectric film 15, a bit line plug 16, bit lines 17, bit line spacers 18, second interlayer dielectric films 19 and a contact plug 20 are sequentially formed on a semiconductor substrate 11 in which a device isolation film 12 is formed, through a common process.

10 As mentioned above, In a multi-layer metal structure system such as DRAM, further, a method by an insulating spacer (word line spacer or bit line spacer) is formed on the sidewall of a metal line using nitride or oxide in order to insulate the metal lines (bit lines or word lines) and a metal plug (bit line plug or contact plug), has been widely used, which thus requires a higher
15 integration of the device and further reduces the distance between the metal lines.

Figs. 4A and 4B are cross-sectional views of the device for explaining a gap filling problem depending on an increased aspect ratio;

Referring to Fig. 1 and Fig. 4A, in order to manufacture a DRAM, a
20 word line 13, a word line spacer 14, a first interlayer dielectric film 15, a bit line plug 16, bit lines 17 and bit line spacers 18 are formed on a semiconductor substrate 11 in which a device isolation film 12 is formed, through a common process.

At this time, the distance "W" between the bit lines 17 is reduced by

the width "L" of the bit line spacer, so that an actual distance "W" between the bit lines is "W-2L".

Referring to Fig. 1 and 4B, with the bit lines 17 and the bit line spacer 18 formed, a second interlayer dielectric film 19 is formed on the entire surface for an electrical insulation with upper elements.

At this time, as the aspect ratio between the bit lines 17 is increased by the bit line spacer 18 and the speed where the second interlayer dielectric films 19 are formed below between the bit lines 17 is therefore further faster than that where the second interlayer dielectric films 19 are formed over the bit lines 17, voids A are generated below between the bit lines 17. This degrades an electrical characteristic of the device and reliability of the process.

SUMMARY OF THE INVENTION

The present invention is contrived to solve the above problems and an object of the present invention is to provide a method of forming an interlayer dielectric film in a semiconductor device, which can improve a burial characteristic between metal lines, in a way that an insulating film spacer is selectively formed only at a region where a plug is formed between the metal lines and the insulating film spacer at a region where the plug is not formed is removed to lower the aspect ratio between the metal lines.

In order to accomplish the above object, a method of forming an interlayer dielectric film in a semiconductor device according to a first embodiment of the present invention is characterized in that it comprises the steps of forming conductive layer patterns of a given pattern and an insulating

film spacer on the sidewalls of the conductive layer patterns through a common process; removing the insulating film spacer formed in a region other than a region where a contact plug will be formed; and forming an interlayer dielectric film on the entire surface.

5 A method of forming an interlayer dielectric film in a semiconductor device according to a second embodiment of the present invention is characterized in that it comprises the steps of forming conductive layer patterns of a given pattern through a common process; forming an interlayer dielectric film on the entire surface; and removing the interlayer dielectric film
10 at a region where a contact plug will be formed and then forming an insulating film spacer on the sidewall of the conductive layer patterns.

 A method of forming an interlayer dielectric film in a semiconductor device according to a third embodiment of the present invention is characterized in that it comprises the steps of forming conductive layer
15 patterns of a given pattern and an insulating film spacer on the sidewall of the conductive layer patterns through a common process; burying a conductive material between the conductive layer patterns; removing the conductive material only at a given region and remaining the conductive material at remaining regions to form a contact plug; and burying an interlayer dielectric
20 film between the conductive layer patterns at a region from which the conductive material is removed.

 In the above, the conductive layer patterns may be word lines or bit lines.

BRIEF DESCRIPTION OF THE DRAWINGS

The aforementioned aspects and other features of the present invention will be explained in the following description, taken in conjunction with the accompanying drawings, wherein:

5 Fig. 1 shows a layout of a general DRAM device;

 Figs. 2A ~ 2C are cross-sectional views of the device taken along lines A-A', B-B' and C-C' in Fig. 1;

 Figs. 3A ~ 3C are cross-sectional views of the device taken along lines A-A', B-B' and C-C' in Fig. 1;

10 Figs. 4A and 4B are cross-sectional views of the device for explaining a gap filling problem depending on an increased aspect ratio;

 Figs. 5A and 5B show layouts for explaining a method of forming an interlayer dielectric film in a semiconductor device according to one embodiment of the present invention; and

15 Figs. 6A ~ 6C are cross-sectional views of a device for explaining a method of forming an interlayer dielectric film in a semiconductor device according to another embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

20 The present invention will be described in detail by way of a preferred embodiment with reference to accompanying drawings.

 Figs. 5A and 5B show layouts for explaining a method of forming an interlayer dielectric film in a semiconductor device according to one embodiment of the present invention.

Referring now to Fig. 5A, a device isolation film (not shown), a junction region **51a**, word lines **53** and a word line spacer **54** are formed on a semiconductor substrate through a common process. Then, a first photoresist pattern **60** is formed at a region wherein a contact plug will be formed, for the purpose of an electrical insulation with upper elements including a capacitor to be formed in a subsequent process. The first photoresist pattern **60** is formed to sufficiently cover the word line spacer **54** in a region where a contact plug will be formed. Thereafter, an exposed portion of the word line spacer **54** is removed by etch process. Thereby, the word line spacer **54** remains on the sidewall of the word lines **53**, with the contact plug and the word lines **53** having a margin that will not be electrically connected together at a region where the contact plug will be formed. Next, a first interlayer dielectric film (not shown) is formed on the entire surface in order to electrically insulate the word lines **53** and bit lines that will be formed in a subsequent process. The word line spacer is removed from remaining regions other than a region that the contact plug will be formed so that the distance between the word lines **53** can be sufficiently secured to lower the aspect ratio. Therefore, the first interlayer dielectric film can be easily buried between the word lines **53** without any voids. As the first interlayer dielectric film must be removed from the region where the word line spacer **54** remains in order to form the contact plug in a subsequent process, there is no problem even when voids are generated in the first interlayer dielectric film in this region. After the word line spacer is removed, the first photoresist pattern **60** is removed.

Referring now to Fig. 5B, a bit line plug (formed below the bit line, not

shown), bit lines 57 and a bit line spacer 58 are sequentially formed at a given region on the first interlayer dielectric film (not shown) formed on the entire surface, through a common process. For the purpose of an electrical isolation with upper elements including a capacitor to be formed in a subsequent process, a second photoresist pattern 61 is formed at a region where the contact plug will be formed. The second photoresist pattern 61 is formed to sufficiently cover the bit line spacer 58 in the region where the contact plug will be formed. The exposed bit line spacer 58 is then removed by etch process. Thereby, the bit line spacer 58 remains on the sidewall of the bit lines 57, with the contact plug and the bit lines 57 having a margin that will not be electrically connected together at a region where the contact plug will be formed. Next, a second interlayer dielectric film (not shown) is formed on the entire surface in order to electrically insulate the bit lines 57 and upper elements including a capacitor that will be formed in a subsequent process. The bit line spacer is removed from remaining regions other than a region that the contact plug will be formed, so that the distance between the bit lines 57 can be sufficiently secured to lower the aspect ratio. Therefore, the second interlayer dielectric film can be easily buried between the bit lines 57 without any voids. Similarly, as the second interlayer dielectric film must be removed from the region where the bit line spacer 58 remains in order to form the contact plug in a subsequent process, there is no problem even when voids are generated in the second interlayer dielectric film in this region. After the bit line spacer is removed, the second photoresist pattern 61 is removed.

Thereafter, though not shown in the drawings, the second and first

interlayer dielectric films are removed to expose the junction region of the semiconductor substrate. Then, a conductive material is buried to form the contact plug and upper elements including the capacitor are formed through a common process.

5 The above process forms an insulating film spacer at the sidewall of the word lines or the bit lines, removing the insulating film spacer in a region where the plug is not formed and buries the interlayer dielectric film, thus securing the distance between the word lines or the bit lines to improve a burial characteristic of the interlayer dielectric film.

10 Also, another embodiment for securing the distance between the word lines or the bit lines by removing an insulating film spacer in a region where the plug is not formed will be below explained.

 After the word lines or the bit lines are formed through a common process, an interlayer dielectric film is completely buried between the word
15 lines or the bit lines before an insulating film spacer is formed. At this time, as the distance between the word lines or the bit lines is sufficiently secured since the insulating film spacer is not formed, between the word lines or the bit lines can be easily buried using the interlayer dielectric film without voids. Thereafter, after only an interlayer dielectric film in a region where the plug
20 will be formed is removed, an insulating film spacer is formed on the sidewall of the word lines or the bit lines, which is exposed by the removed interlayer dielectric film.

 In addition, still another embodiment for securing the distance between the word lines or the bit lines by removing an insulating film spacer in a region

where the plug is not formed will be below explained.

Figs. 6A ~ 6C are cross-sectional views of a device for explaining a method of forming an interlayer dielectric film in a semiconductor device according to another embodiment of the present invention.

5 Referring now to Fig. 6A, word lines (not shown), a word line spacer (not shown) and a junction region (not shown) are formed on a semiconductor substrate 71 in which a device isolation region 72 is formed at a given region, through a common process. Then, a first interlayer dielectric film 73 is formed on the entire surface. After the first interlayer dielectric film 73 on
10 the junction region is removed by etch process, a conductive material is buried into a region from which the first interlayer dielectric film 73 is removed to form a first contact plug 74, in order to electrically connected the junction region and upper elements to be formed in a subsequent process. Next, insulating films of a given pattern such as bit lines 75 and a nitride film 76 are
15 sequentially formed on the first interlayer dielectric film 73 and an insulating film spacer 77 is then formed on the sidewall of the bit line 75 and the nitride film 76. At this time, an upper surface of the first contact plug 74 is exposed between the bit lines 75. Then, after polysilicon or a conductive material is formed on the entire surface, polysilicon or the conductive material on the
20 nitride film is removed by means of planarization process, so that it remains only between the bit lines 75, thus forming a second contact plug 78. If the second contact plug 78 is formed between the bit lines 75, a photoresist pattern 79 of a given pattern is formed on the entire surface to expose only an unnecessary portion of the second contact plug.

Referring now to Fig. 6B, the unnecessary portion of the second contact plug is removed by etching process and the exposed insulating film spacer 77 is removed while the second contact plug is removed. Then, the photoresist pattern is removed.

5 Thereby, the second and first contact plugs 78 and 74 electrically connect an upper element such as a capacitor, etc., that will be formed in a subsequent process, to the junction region.

Referring now to Fig. 6C, a second interlayer dielectric film 80 is formed on the entire surface. Then, a planarization process such as chemical
10 mechanical polishing process, and the like is implemented to bury the second interlayer dielectric film 80 between the bit lines 75 from which the second contact plug and the insulating film spacer are moved to electrically isolate the bit lines 75.

The insulating film spacer is removed from between the bit lines 75 in
15 which the second interlayer dielectric film 80 is buried, thus lowering the aspect ratio. Therefore, the second interlayer dielectric film 80 can be easily buried without voids.

Though the above methods can easily bury an insulating material between word lines or bit lines having a narrow width in a memory device,
20 they can also easily bury the insulating film between metal lines or patterns having a narrow width.

As mentioned above, the present invention can easily bury an insulating material between metal lines without voids by selectively forming an insulating film spacer only at a given region. Therefore, the present

invention has an advantage that it can improve reliability of the process and an electrical characteristic of the device.

The present invention has been described with reference to a particular embodiment in connection with a particular application. Those having
5 ordinary skill in the art and access to the teachings of the present invention will recognize additional modifications and applications within the scope thereof.

It is therefore intended by the appended claims to cover any and all such applications, modifications, and embodiments within the scope of the
10 present invention.